PLL LOCK DETECTION CIRCUIT USING EDGE DETECTION

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ABSTRACT

A lock detection circuit operatively associated with a phase-locked loop indicates when a feedback clock signal is locked to a reference clock signal. The lock detection circuit counts the number of rising and falling edges of the feedback clock signal that are detected between rising edges of the reference clock cycle. The lock detection circuit counts the number of consecutive valid cycles of the reference clock signal during which a single rising edge and a single falling edge of the feedback clock signal are detected. Lock detection circuit asserts a lock signal when the number of consecutive valid cycles counted exceeds a predetermined number. Where the lock detection circuit indicates locked signals and then detects a reference clock cycle that is not valid, lock detection circuit continues to indicate lock if the next reference clock cycle is valid relative to a skewed feedback clock signal.